REMARKS

Prior to entry of this paper, Claims 1-20 were pending. Claim 5 was objected to. Claims 1-4 and 6-20 were rejected. In this paper, no claims have been amended, cancelled, or added. Accordingly, Claim 1-20 are currently pending. For at least the following reasons, the applicants' representative respectfully submits that each of the presently pending claims is in condition for allowance.

Allowable Subject Matter (Claim 5)

Independent Claim 5 was objected to for being dependent on a rejected base claim, but indicated to be allowable if re-written in independent form. This objection is respectfully traversed. The applicants' representative respectfully submits that the objection to Claim 5 should be withdrawn. Claim 5 is independent, and was prior to entry of this paper. For at least this reason, it is respectfully submitted that Claim 5 is in condition for allowance.

Claims 1, 9, 13-14, 18, and 20

Claims 1, 9, 13-14, 17-18, and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Publication No. 2002/0067773 to Jackson et al. ("Jackson"). Claims 7, 8, and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson. Each of these rejections is respectfully traversed.

Claim 1 is respectfully submitted to be allowable at least because Jackson fails to disclose, "the synthesized signal is a clock signal," as recited in the applicants' Claim 1.

The applicants' representative respectfully submits that clock signals are typically in the form of a square wave, having a waveform shape that is generally repeated every clock cycle. The signal output by VCO 64 of Figure 3 of Jackson is not a clock signal for at least the reason that the waveform shape of this signal is not repeated every clock cycle. Rather, this signal is a phase-modulated sinusoid having a waveform shape that changes based on *serial data* that is encoded into the signal (i.e., modulated according to offset quadrature phase-shift keying (OQPSK) modulation).

According to Jackson, the modulator 30 of Figure 3 has an input port 34 "for receiving *serial data* to be transmitted." (Jackson, ¶20; Emphasis added). Jackson's OQPSK modulator 81 outputs a digital data modulation signal "representing the modulation that needs to be imposed on [a] carrier signal such that the resulting modulated carrier signal represents *the serial input data* offset QPSK modulated." (Jackson, ¶27; Emphasis added). Jackson employs frequency modulator 82 and PLL 33 of Figure 3 to output the carrier signal according to the frequency value of Jackson's digital data modulation signal.

In the ***Response to Arguments***, the Office Action argues that VCO's employed in PLLs inherently produce clock signals, "[i]t is well known in the art that a VCO in PLL synthesizer is a clock signal." (Office Action, page 2). The applicants' representative respectfully disagrees and submits that the Office Action has not provided rationale or evidence tending to show this inherency regarding VCO's employed in PLLs. (see MPEP 2112).

In fact, the Jackson reference provides evidence that is contrary to the Office Action's position. As discussed above, Jackson discloses that the output of PLL 33 of Figure 3 (provided by VCO 64) is representative of *serial data* that has been OQPSK modulated onto a carrier signal.

Further, in the ***Response to Arguments***, the Office Action also argues that a sinusoidal signal is inherently a clock signal, (Office Action, page 2). However, "[t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." (MPEP 2112). Although a sinusoidal signal can in some instances be a clock signal, a person skilled in the art would appreciate that a sinusoidal signal has a high timing uncertainty, and therefore a sinusoidal signal is typically not construed to be a clock signal unless treated in a special manner (e.g., employed differentially to increase slew rate).

The rejection to Claim 1 should also be withdrawn at least because Jackson fails to disclose, "wherein the spread spectrum clock generator is arranged such that the output clock signal is a clock signal that is a spread-spectrum signal," as presently recited in the applicants' Claim 1.

Rather, Jackson's modulator 30 outputs a linearized OQPSK modulator signal. According to Jackson, the PLL 33 of Figure 3 is continually adjusted "such that the output signal generated by the PLL 33 is frequency modulated in accordance with the output signal of the OQPSK modulator 81." (Jackson, ¶28). Accordingly, the output signal of the of Jackson's modulator 30 is

at most an OQPSK modulated signal. A person skilled in the art would understand this to mean that the output signal has been phase-shifted such that each phase shift is indicative of one of four phase symbols (i.e., to discriminate between individual sets of bits of the serial data input at input 34 of Figure 3).

However, a person skilled in the art would not construe Jackson's linearized OQPSK signal to be spread spectrum. A spread spectrum signal has a reduced amplitude carrier with sideband harmonics (see, e.g., Specification, pg. 1, lines 29-31). Consequently, the resultant spread spectrum signal has a wider bandwidth relative to a signal that is not spread spectrum. Jackson's does not employ spread spectrum for at least the reason that Jackson's goal is to reduce the bandwidth of the linearized OQPSK signal, "the modulator 30 is able to achieve linearized OQPSK modulation, which allows for *a reduction in the necessary bandwidth* of the transmitted signal." (Jackson, ¶23; Emphasis added).

Claim 7 is respectfully submitted to be allowable at least because it depends from Claim 1.

Claim 9 at least because Jackson fails to disclose, "a clock divider circuit that is configured to provide an output clock signal from the synthesized clock signal," as recited in the applicants' Claim 9.

In the ***Response to Arguments***, the Office Action argues that the output signal from a VCO is a clock signal, and "[t]herefore, the clock divider circuit does provide an output clock signal." The applicants' representative respectfully disagrees. As discussed above, Jackson's VCO 64 does not output a clock signal, but rather serial data that is encoded onto a sinusoid.

In addition, assuming arguendo that Jacksons' variable divider 20 of Figure 1 reads on the adjustable clock divider circuit of Claim 9, Jackson does not disclose a separate clock divider that receives a signal from the VCO 18 of Figure 1.

Claims 13 and 20 are respectfully submitted to be allowable at least for reasons similar to those stated above with regard to Claim 1. Claims 14, 17, and 18 are respectfully submitted to be allowable at least because they depend from Claim 13.

Claims 2-4, 6, 8, 10-12, 15, 16, and 19

Claims 2 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson in view of U.S. Patent No. 4,182,988 to Murakami ("Murakami"). Each of these rejections is respectfully traversed, and the applicants' representative respectfully submits that Claims 2 and 5 are allowable for at least the reason that they depend from one of Claims 1 and 13.

Claim 3 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson in view of U.S. Publication No. 2003/0058053 to Jeon et al. ("Jeon"). This rejection is respectfully traversed, and the applicants' representative respectfully submits that Claim 3 is allowable at least because it depends from Claim 1.

Claims 4 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson as applied to claim 1 above, and further in view of U.S. Patent No. 6,760,571 to Prockup ("Prockup"). Each of these rejections is respectfully traversed, and the applicants' representative respectfully submits that Claims 4 and 16 are allowable for at least the reason that they depend from one of Claims 1 and 13.

Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson as applied to claim 1 above, and further in view of U.S. Publication No. 2003/0053577 to Watarai ("Watarai"). This rejection is respectfully traversed, and the applicants' representative respectfully submits that Claim 6 is allowable at least because it depends from Claim 1.

Claims 10 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson, in view of U.S. Patent No. 5,152,005 to Bickley ("Bickley"). Each of these rejections is respectfully traversed, and the applicants' representative respectfully submits that Claims 10 and 19 are allowable for at least the reason that they depend from one of Claims 9 and 18.

Claims 11 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson, in view of Leung et al. (U.S. Patent No. 6,580,432), hereinafter "Leung". Each of these rejections is respectfully traversed. The applicants' representative respectfully submits that Claim 11 is allowable for at least the reason that it depends from Claim 1.

Claim 12 is respectfully submitted to be allowable at least because Jackson or Leung fail to teach or suggest "wherein the modulating waveform is suitable for spreading a frequency spectrum

that is associated with the synthesized signal relative to a frequency spectrum that is associated with the reference signal," as recited in the applicants' Claim 12.

In the ***Response to Arguments***, the Office Action states, "[t]he issue is not a matter of the circuit being operable or inoperable, since Leung is being used to fill the gap in order to solve the problem." (Office Action, page 3).

The applicant's representative respectfully disagrees and submits that the proposed modification of Jackson based on Leung would corrupt the data encoded in Jackson's linearized OPQSK signal. Therefore, the proposed modification would render the circuit of Jackson unsuitable for its intended purposes. "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." (MPEP 2143.01). The applicants' representative appreciates that the test for obviousness here is not whether the specific features of Leung may be bodily incorporated into the structure of Jackson. Rather, "the test [for obviousness] is determined by what the combined teachings of those references would have suggested to those of ordinary skill in the art." (MPEP 2145, III). "However, the claimed combination cannot change the principle of operation of the primary reference or render the reference inoperable for its intended purpose." (MPEP 2145, III).

Here, Jacksons' intended purpose is to offset QPSK modulate an input signal (Jackson, ¶9). Lueng discloses a technique in which a spread spectrum clock signal and another clock signal adjust an output frequency of data read from a spread-spectrum FIFO (Leung, Abstract). A person skilled in the art would appreciate that the encoding of Jackson's input signal would be corrupted if carried out in the manner with which Leung adjusts output frequency. Therefore, the operablilty of the proposed combination of Jackson and Leung is an issue.

Jackson's modulator 33 of Figure 3 outputs a linearized OPQSK modulator signal, which is based on the digital data modulation signal provided by Jackson's offset QPSK modulator 81 of Figure 3 (Jackson, ¶27). This digital data signal provides a specific encoding for the linearized OPQSK signal. Further modulating this digital data signal in the manner of Leung would corrupt the data encoded in the linearized OPQSK signal.

CONCLUSION

It is respectfully submitted that each of the presently pending claims are in condition for allowance and notification to that effect is requested. The Examiner is encouraged to contact the applicants' representative at the below-listed telephone number if it is believed that the prosecution of this application may be assisted thereby. Although only certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentable. The applicants reserve the right to raise these arguments in the future.

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